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Real Processing-in-Memory with Memristive Memory Processing Unit

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Computers have been built for many years in a structure where data is processed and stored using separate units – the processor and the memory. However, emerging applications such as artificial intelligence and internet-of-things require ample amount of data to be processed from numerous origins. This forces enormous data movement that becomes the main limitation in modern computing systems. Not only that the speed of computers is limited by this data movement, but also the energy consumption is mostly because of this transfer rather than the computation itself.

An attractive approach to alleviate the data movement problem is to process data inside the memory. Unfortunately, contemporary memory technologies are ill-suited for such approach. Memristive technologies are attractive candidates to replace conventional memory technologies, and can also be used to perform logic and arithmetic operations. Combining data storage and computation in the memory array enables a novel computer architecture, where both operations are performed within a memristive Memory Processing Unit (mMPU). mMPU relies on adding computing capabilities to the memristive memory cells without changing the basic memory array structure, and by that overcome the primary restriction on performance and energy in computers today.

This talk focuses on the various aspects of mMPU. I will discuss its architecture and implications on the computing system and software, as well as examining the microarchitectural aspects. I will show how to design the mMPU controller and how different sequence of computing operations in an mMPU can be automatically optimized as sequences of basic Memristor Aided Logic (MAGIC) NOR and NOT operations. Then, I will present examples of applications that can benefit from processing within memristive memory and show how adding mMPU to conventional computing systems substantially improves the system performance and energy.

Biography

Shahar Kvatinsky is an assistant professor at the Andrew and Erna Viterbi Faculty of Electrical Engineering, Technion – Israel Institute of Technology. He received the B.Sc. degree in computer engineering and applied physics and an MBA degree in 2009 and 2010, respectively, both from the Hebrew University of Jerusalem, and the Ph.D. degree in electrical engineering from the Technion – Israel Institute of Technology in 2014. From 2006 to 2009 he was with Intel as a circuit designer and was a post-doctoral research fellow at Stanford University from 2014 to 2015. Kvatinsky is an editor in Microelectronics Journal and has been the recipient of the 2015 IEEE Guillemin-Cauer Best Paper Award, 2015 Best Paper of Computer Architecture Letters, Viterbi Fellowship, Jacobs Fellowship, ERC starting grant, the 2017 Pazy Memorial Award, the 2014 and 2017 Hershel Rich Technion Innovation Awards, 2013 Sanford Kaplan Prize for Creative Management in High Tech, 2010 Benin prize, and six Technion excellence teaching awards. His current research is focused on circuits and architectures with emerging memory technologies and design of energy efficient architectures.